Firmware /FREQ

The /FREQ firmware is a comfortable 9-MHz frequency counter with additional features, like digital I/O, PWM output, pulse and clock generator and six ADC channels.

Digital-I/O
All I/O lines have a fixed data direction, that can not be changed. All lines use TTL levels (5V) and can be used as digital input or output, depending on their direction. Lines overtake alternative functions depending on the application and configuration, but they never change their direction.

9-MHz frequency counter
D2 and D5 are used as frequency measure inputs. Usually the input signal gets connected to BOTH inputs (bind together). The measurement principle changes automatically depending on the input frequency. High frequencies are measured by edge counting during a gate time interval (D5; F>250 Hz). Low frequencies are measured by edge detection and measurement (D2; F<250 Hz).

Gate time intervals can be 2000ms / 1000 ms / 500ms / 100 ms / 50 ms / 20 ms / 10ms.
The gate clock can be output through digital output D7

For low frequency signals (< 250 Hz) the elapsed time since last falling edge on D2 is measured and reported. Frequency measurement, counter function and time measurement can be used for low frequencies simultaneously. For high frequencies only frequency measurement and counter function are available alternatively.

32-bit counter
With gate time generator deactivated, the frequency counter works as simple 32-bit up counter, counting falling edges at D5. Digital input B0 can be configured as external RESET input for the counter. Digital input B4 can be configured as external ENABLE input for the counter.

Generator 1
A periodic output signal is generated at digital output D6. An input clock drives a internal 8 bit counter. The counter value gets compared and the compare result generates the output clock at D6. Depending on the configuration the output signal can be a clock with adjustable frequency or pulse width,

The input clock signal can be internal or external.

Internals clock sources are devided system clocks (18.432000 MHz) with divisors of 1, 8, 64, 256 or 1024. Input D4 can be configured as external ENABLE input for the internal clock source.

External clocks are supplied through input D4 as well. External clocks at D4 can be enabled or disabled by software.

Generator 2
A pulse with adjustable pulse length is output at D3.

Duration of HIGH and LOW signal output is adjusted separately in multiples of a common time base value (16 bits resolution). Available time bases are 125µs, 500µs, 5ms und 500 ms.

The output pulse can be generated continuously or single shot. A single shot can be triggered by software. Digital input B1 can be configured and used as trigger as well.
In continuous mode a trigger will cause the output clock to synchronize with the trigger (software or B1).

Generator 3
A adjustable (8 bit) PWM signal with a fixed frequency of 72kHz is generated at digital output D3.

Connections

B0 Digital Input (Counter RESET)
B1 Digital Input (Sync/Trigger Generator 2)
B2 Digital Output
B3 Digital Output (Generator 3 PWM)
B4 Digital Input (Counter enable)
B5 Digital Output (LED)

D2 Diigtal Input (Frequency input 0-250Hz)
D3 Digital Output (Generator 2)
D4 Diigtal Input (EXT CLK ENABLE)
D5 Diigtal Input (Frequency input 250 Hz - 8MHz)
D6 Digital Output (Generator 1)
D7 Digital Output (Gate Clock Output)

C0…C5 Digital Inputs / ADC 0…5

Inputs of Port B and Port D are pulled up to Vcc internally. Port C provides digital inputs without pull-ups. Voltages at port C can be read with the internal ADC. The reference voltage for the ADC can be taken from three different sources:

External reference voltage:
A individual reference voltage is supplied trough the VREF input (0<Vref<Vcc).

Internal reference voltage VCC
The positive supply voltage (Vcc) is used as reference voltage. (approx. 5V)

Internal reference voltage 1.1 V
A 1.1 Volt reference is generated internally.

Protocol description

Baud 57600
8 data bits
No parity
1 stop bit

Request / Response communication is used. A request consists of 10 data bytes. After receiving 10 bytes, the device responses with a 33 bytes long response data block

Request: 10 Bytes

The request data block is 10 bytes long and transfers all control data.

Byte 1 Gate time and Digital Out

Bits 0..2 select the gate time interval fort he frequency measurement:

Bit 210	Hex	Dec	Gate time
000	00h	0	2 s
001	01h	1	1s
010	02h	2	500 ms
011	03h	3	100 ms
100	04h	4	50 ms
101	05h	5	20 ms
110	06h	6	10 ms
111	07h	7	OFF / COUNTER

Bits 3…7 are assigned to the digital outputs B2, B3, B5, D3 and D6, one after each other. These bits control the output state and activate alternative functions for the corresponding output.

Byte 2 Compare value for generator 1

This byte adjust the compare value of generator 1 and varies output frequency or PWM depending on the generator mode.

Byte 3 Compare value generator 3

This byte adjust the compare value of generator 3 and varies PWM.

Byte 4 Mode

Following functions are encoded in byte 4 bitwise:

- Mode and clock source for generator 1
- Time base for generator 2
- Counter reset by software

The value for byte can be calculated, adding up the decimal of HEX values of the desired functions.

Bits 0…2 select the clock source for **generator 1**.

Bit [210]	Hex	Dec	Clock source	
000	00h	0	NONE	
001	01h	1	CLK	18.432000 MHz
010	02h	2	CLK / 8	2.304000 MHz

011	03h	3	CLK / 64	288.000 KHz
100	04h	4	CLK / 256	72.000 KHz
101	05h	5	CLK / 1024	18.000 KHz
110	06h	6	EXTERNAL CLOCK (D4), falling edge	
111	07h	7	EXTERNAL CLOCK (D4), rising edge	

Bit 3 resets the (frequency) counter to zero (**Counter Software Reset**), if bit is SET.

Bit	Hex	Dec	
[3]	08h	8	Counter Reset

Bit 4 and Bit 5 select the **mode of generator 1**

Bit [54]	Hex	Dec	Mode Generator 1
00	00h	0	Normal
01	10h	16	PWM
10	20h	32	CTC
11	30h	48	Fast PWM

Mode: Normal
The generator devides the input frequency by 512.

Fout = (Fin / 2) / 256

Fixed output frequencies with internal clock source:

36.000 kHz
4.500 kHz
562,5 Hz
140,625 Hz
35,15625 Hz

Mode: PWM
The generator devides input frequency by 2 and by 255 after that.
The pulse width is varies with the compare value.

Fout = (Fin / 2) / 255

PWM frequencies with internal clock sources:

36.141 kHz
4.518 kHz
564,7 Hz
141,17 Hz
35,294 Hz

Modus: CTC
The input frequency is devided by 2 and then devided by compare value +1.
So the output frequency varies with the compare value.

Fout = (Fin / 2) / (CMP1 + 1)

Frequency ranges with internal clock sources:

36.141 kHz – 9.216 MHz
4.518 kHz – 1.152 MHz
564,7 Hz - 144.0 kHz
141,17 Hz - 36.0 kHz-
35,294 Hz – 9.0 kHz

Modus: Fast PWM
The input frequency is devided by 256.
The pulse width is varies with the compare value.

Fout = Fin / 256

PWM frequencies with internal clock sources:

72.000 kHz
9.0 kHz
1.125 kHz
281,25 Hz
70,3125 Hz

Bit 6 und Bit 7 select the **time base for generator 2** ein.

Bit [76]	Hex	Dec	Time base Generator 2
00	00h	0	125 µs
01	40h	64	500 µs
10	80h	128	5 ms
11	C0h	192	500 ms

Byte 5…6 TH; Generator 2 ; Duration HIGH (INT16 / WORD)
Byte 7…8 TL; Generator 2; Duration LOW (INT16 / WORD)

Two bytes make up a 16 bit value, which sets the pulse HIGH/LOW duration of generator 2.
Time is the result of the multiplication of the duration value and the tme base value:

T high [s] = TH * Time base
T low [s] = TL * Time base

With TH = TL = 1 and time base = 125µs we get the
maximum output frequency of 4 kHz. f = 1/ ((TL + TH) * Time base)

With TH = TL = FFFFh and time base = 500ms we get the
maximum period length of 65535 seconds, which is more than 18 hours
T = (TL + TH) * time base

Byte 9 Configuration And Digital Out (Flags)

Bits in this Byte are flags for some configurations and functions.

Bit 0 If Bit 0 is SET, B0 becomes RESET input for the (frequency) counter.
Bit 1 If Bit 1 is SET, B1 becomes SYNC/TRIGGER input for generator 2.
Bit 2 If Bit 2 is SET, B4 becomes ENABLE input for the (frequency) counter.
Bit 3 Bit 3 sets the mode of generator 2: Continuous / Single-shot
Bit 4 Bit 4 is SYNC/TRIGGER for generator 2 (software trigger)
Bit 5 In case of **external** clock source for generator 2:

Bit 5 SET enables the clock input from D4
Bit 5 CLEAR disables the clock input from D4
In case of **internal** clock source for generator 2:
Bit 5 SET: D4 is enable input for internal clock.
Bit 5 CLEAR: Internal clock enabled; independent from D4

Bit 6 Bit 6 activates Gate Clock Output at D7.
Bit 7 Bit 7 turns output D7 on/off.

Byte 10 ADC reference selection (VREF SELECT)

Bit 0..1 select the reference voltage source for the ADC conversion (C0…C5)

Bit 10	Hex	Dec	VREF
00	00h	0	External from VREF terminal
01	01h	1	Internal (Vcc)
10	02h	2	undefined
11	03h	3	Internal 1.1 Volt

Bit 2..7	Reserved	Set to zero

Response: 33 Bytes

The device sends a 33 Byte response after a 10 Byte request.

Byte 1…4 Edge measurement T1 (INT32 / DWORD)
Byte 5…8 Edge measurement T2 (INT32 / DWORD)
Byte 9…12 Edge measurement T3 (INT32 / DWORD)

Four bytes make up an 32 bit value (LSB first).
Three words T1, T2 and T3 deliver the result of the edge measurement. A falling edge on D2 triggers the readout of a free running 32 bit counter, while the counter is clocked with a fixed 72kHz clock (T = 13,8µs). The readout result is reported in data word T2, while the previous readout value is shifted to data word T1.

The signal frequency and period can be calculated as follows:

T = (T2 – T1) * 13,8 µs
F = 1 / T

As the counter will overflow at $FFFFFFFF and start from zero, it is recommended checking the T2>=T1 condition.

Data word T3 is filled with the current counter value. So the difference (T3-T2) delivers the time elapsed since last falling edge at D2.

T elapsed = (T3 – T2) * 13,8 µs

Check T3>=T2 condition.

Byte 13…16 Frequency counter / Counter CNT (INT32 / DWORD)

Four bytes make up an 32 bit value (LSB first). The data word CNT contains a counter value of the 32 bit counter clocked from D5. In case a gate time is activated, the CNT value is readout from the counter when gate time elapses and the counter is reset. (For calculation of frequency: see Byte 20)

If no gate time is active the data word contains the current counter value.

Byte 17 Digital state Port B (Byte)

Bits 0..5 indicate the digital state of lines B0…B5.

Byte 18 Digital state Port C (Byte)

Bits 0..5 indicate the digital state of lines C0…C5.

Byte 19 Digital state Port D (Byte)

Bits 2..7 indicate the digital state of lines D20…D7.

The digital state is independent from the data direction.

Byte 20 Gate time GT [1/100 s]

This byte contains the gate time (in 1/100 s units) that was active for above CNT value.

Frequency at D5 can easily be calculated by software:

F [Hz] = CNT / (GT / 100)

If no gate time is active, a frequency can not be calculated, as GT is zero.

Byte 21..22 ADC0 (Word)

Byte 23..24 ADC1 (Word)
Byte 25..26 ADC2 (Word)
Byte 27..28 ADC3 (Word)
Byte 29..20 ADC4 (Word)
Byte 31..32 ADC5 (Word)

Bytes 21...32 are paired to six words, containing the 10 bit conversion results of the ADC channels (Port C0…C5). Voltage can be calculated as follows:

Voltage = VREF * (MSB * 256 + LSB) / 1023

U0 [Volt] = ADC0 / 3FFh * Vref

Byte 33 Reserved

Byte 33 is reserved and currently 13.